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Simulation shows delay in switch turning off. • gate drive **parasitic** impedance

Simulation of loop gain provides validation of chosen **component** values ...

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... affordable co-**simulation** to designers of traditional RF board and microwave

components. The ... coupling and **parasitic** effects makes Momentum GX an ... can be

used inside Genesys for co-**simulation** with **circuit** elements. ...

[www.home.agilent.com/agilent/redirector.jsp?ckey...action...](#)

[Simulation and Fabrication of Embedded Capacitors in the ...](#)

by YOU Hee-Wook - 2008 - [Related articles](#)

circuit board. All embedded capacitors which employed in ... applications, and the

inductance is the **parasitic component** to be removed. ...

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the omission of **parasitic circuit** elements which may have an important influence on the

circuit analysis code, however, other **circuit simulation** codes ...

[portal.acm.org/ft_gateway.cfm?id=804830&type=pdf](#)

[EDA Focus December 2009: Synopsys Pushes into RFICs | November 30 ...](#)

Dec 2, 2009 ... Extracted Models and **Circuit Simulation** ... Some of these structures are so

small that tiny absolute errors in **parasitic** capacitance are large percentage errors ...

StarRC Custom is one **component** in an expanded Synopsys ...

[www.mwjournal.com/News/article.asp?HH_ID=AR_8412](#) - [Cached](#)

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by KS Kundert - [Cited by 3](#) - [Related articles](#) - [All 5 versions](#)

Try to **disable** the oscillator before using this method. careful to avoid very small

parasitic resistances. ... Second, the **simulator** may add **components** to the **circuit** that

the user did not explicitly spec-ify, such as gmin. ...

[www.kenkundert.com/docs/eda%2B%93-paper.pdf](#)

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System vs. **circuit simulation**. Advantages of software PLECS ... Power circuit with

manufacturer specific **components**. **Parasitic** effects (magnetic hysteresis) ...

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of **parasitic components** and therefore a predictable transient response. ... Experiments: A set of **simulation** experiments were conducted on defective and ... the transient response of a defective **circuit** are observable at one or more ...
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the **component parasitic** models. To aid in the design, a **circuit simulator** computer program is used to model the circuitry with parasitics. ...
www.ile.rochester.edu/pub/review/v73i2_sweep.pdf

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Lab2 for EE715

Apr 29, 1997 ... **Parasitic** extraction and backannotation with IC verify. we only need to wire up the **devices** using poly, metal1, metal2, via and contact_to_poly. ... In this lab, we will extract for **analog simulation** (AccuSim II)

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Analog/Mixed Signal Simulation

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SPICE is a general purpose **analog simulator** and contains models of circuit elements, such as resistors, capacitors, inductors, and semiconductor **devices**. ...

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parasitic simulation efforts were applied to developing this new methodology. ... instead of the **analog** transistor-level schematics, the **simulation** vastly sped up. when in part of a **device** terminal name. Because we are ...

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UltraSim Simulator User Guide -- 3. Simulation Options

Detect **parasitic** vertical PNP BJT **devices** and invoke aggressive partitioning ... tells the **simulator** to **disable** the **simulation** for all instances of the ...

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It is built upon the production-proven **analog simulation** platform, ... For large **parasitic**-dominant designs, Spectre turbo technology provides a **parasitic** reduction ... of **device** models to remove unneeded and inefficient operations. ...

www.cadence.com/ri/Resourses/white.../spectre_turbo_wp.pdf - [Similar](#)

VOLTAGE LEVEL TRANSLATION - Patent application - virtual zero ...

Load side **parasitic** CMOS input capacitance in this case is ironically an asset rather than ...

3 shows a voltage level translation circuit with realistic **device** models TOPSpice is a commercial **analog simulation** tool developed by PENZAR Corporation. C1 network to enable/**disable** level translation. [0061]4. ...

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Device Simulation of a Trench-IGBT with Integrated Diverter Structures

The ability of a **device simulator** to predict and enable user's to view the electric ... This indicates the latch-up of the **parasitic** thyristor structure ...

www.simucad.com/simulationstandard/1995/dec/a5/a5.html - [Cached](#)

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Response Testing of **Analog** and Digital CMOS Circuits. **Simulation** experiments show that variations in the transient ... Alternatively, **device** defects add or remove **parasitic** elements from the AC network in the region of the defect. ...

www.csee.umbc.edu/vlsi/papers/e_letters.pdf

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device in the schematic, and bring up the "Edit Object Properties" form (Edit->Object- Finally, press Esc for **disabling** the current action. ... structure determines the transconductances of the transistors, the **parasitic** capacitances and Start the **simulation** environment using Tools > **Analog** Environment. ...
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Simulation and modelling of VDMOSFET self protection under TLP ...

by M Sauter - 2009

A scalable model for **analog** circuit **simulation** is developed. ... The **devices** under investigation are DMOSFETs with vertical drift region fabricated in ... the trigger current due to turn on of the **parasitic** bipolar junction transistor. ...
linkinghub.elsevier.com/retrieve/pii/S0026271409003758

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